Appl. No. 10/604,439
Amdt. dated July 06, 2006
Reply to Office action of March 06, 2006

**Amendments to the Claims:**

1. (currently amended) A method for Auxiliary-powered Signal Triggered ~~PCI (Peripheral Component Interconnect) Express~~ Power Management ~~(PM)~~ (ASTPM) ~~(Power Management)~~ using a PCI (Peripheral Component Interconnect) traditional level triggered PM mechanism in a computer system, the computer system including a PCI level triggered PME (Power Management Event) controller and a PCI ASTPM ~~Express~~ Root Complex, the method comprising:

converting an ~~a Beacon~~ auxiliary-powered wakeup signal generated by the PCIASTPM ~~Express~~ Root Complex into a Pseudo-PME signal, the auxiliary-powered wakeup ~~Beacon~~ signal asserting the Pseudo-PME signal so that a voltage of Pseudo-PME signal changes from a first level to a second level;

providing a Pseudo-PME line electrically connecting an output of the PCI ASTPM ~~Express~~ Root Complex with a PME input of the PCI PME controller for transmitting the Pseudo-PME signal to the PCI PME controller, the PME input receiving PME signals generated by other level triggered~~PCI compliant~~ devices ~~through a PCI Bus of the computer system~~; and

before the computer system is under the control of an operating system, de-asserting the Pseudo-PME signal so that the voltage of the Pseudo-PME signal changes from the second level to the first level;

wherein the first level and the second level of the voltage of the Pseudo-PME signal are PCI compliant with the level triggered PME controller.

2. (original) The method of claim 1 wherein the PCI PME controller is a chipset of the computer system.

3. (currently amended) The method of claim 1 further comprising providing a sequential

circuit to convert the auxiliary-powered wakeup ~~Beacon~~ signal into the Pseudo-PME signal.

4. (original) The method of claim 3 wherein the sequential circuit is a latch or a flip flop.

5. (original) The method of claim 1 further comprising providing a timer to control the time interval between asserting and de-asserting the Pseudo-PME signal.

6. (currently amended) The method of claim 1 further comprising converting a pulse of the auxiliary-powered wakeup ~~Beacon~~ signal into a lower frequency pulse to control a time interval between asserting and de-asserting the Pseudo-PME signal.

7. (currently amended) The method of claim 6 further comprising providing a synchronizer to convert the pulse of the auxiliary-powered wakeup ~~Beacon~~ signal into the lower frequency pulse.

8. (original) The method of claim 6 wherein the lower frequency pulse is an active-low pulse and functions as the Pseudo-PME signal in the computer system.

9. (original) The method of claim 1 further comprising utilizing a main power recovery related signal to control a time interval between asserting and de-asserting the Pseudo-PME signal.

10. (original) The method of claim 9 wherein the main power recovery related signal is a PWROK signal of the computer system.

11. (original) The method of claim 9 wherein the main power recovery related signal is a

PSON signal of the computer system.

12. (original) The method of claim 9 wherein the main power recovery related signal is an RST signal of the computer system.

13. (original) The method of claim 9 wherein the main power recovery related signal is a BIOS (Basic Input Output System) driven signal of the computer system.

14. (original) The method of claim 1 wherein the PCI PME controller includes an event register which can be set by the PCI PME controller when the Pseudo-PME signal is asserted but cannot be cleared when the Pseudo-PME signal is de-asserted, the method further comprising clearing the event register with computer code resident in a memory of the computer system.

15. (original) The method of claim 14 wherein the computer code is a device driver of the computer system.

16. (currently amended) A computer system comprising:

a PCI PME controller having a PME input;

a PCI auxiliary-powered Signal Triggered Power Management (ASTPM) ~~Express~~ Root Complex having an output for outputting a generated Beacon signal;

a sequential circuit electrically connected to the output of PCI ASTPM ~~Express~~ Root Complex, the sequential circuit having an output for outputting a Pseudo-PME signal of a first voltage level or a second voltage level according to the Beacon signal; and

a Pseudo-PME line electrically connecting the output of the sequential circuit to the PME input of the PCI PME controller;

wherein the first voltage level and the second voltage level are PCI compliant with

the level triggered PME controller.

17. (currently amended) The computer system of claim 16 wherein when the sequential circuit inputs a Beacon signal from the PCI ASTPM ~~Express~~-Root Complex, the Pseudo-PME signal is changed from the first voltage level to the second voltage level.

18. (original) The computer system of claim 17 further comprising a timer connected to the sequential circuit to control when the Pseudo-PME signal is changed from the second voltage level to the first voltage level.

19. (original) The computer system of claim 17 wherein a main power recovery related signal is utilized to control when the Pseudo-PME signal is changed from the second voltage level to the first voltage level.

20. (original) The computer system of claim 17 wherein the PCI PME controller further comprises an event register, the event register being set when the Pseudo-PME signal is changed from the first voltage level to the second voltage level, and the computer system further comprises a memory comprising computer code executed by the computer system when the Pseudo-PME signal changes from the second voltage level to the first voltage level, the computer code clearing the event register.